Notice of Allowability	Application No. 10/767,273	Applicant(s) LEE ET AL.	
	Examiner James K. Trujillo	Art Unit 2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *interview dated 25 August 2004*.

2. ☒ The allowed claim(s) is/are *187 and 189-196 (renumbered as 1-9)*.

3. ☒ The drawings filed on *30 January 2004* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 01302004
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *08252004* .
7. ☐ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

1. The office acknowledges the receipt of the following and placed of record in the Application file dated 1/30/04.

2. Claims 187-196 are presented for examination file.

Allowable Subject Matter

3. Claims 187 and 189-196 are allowed.

REASONS FOR ALLOWANCE

4. The following is an examiner's statement of reasons for allowance:

Li et al., U.S. Patent 6,691,214 (hereinafter "Li") teaches a device comprising a functional circuit, said functional circuit comprising: a logic circuit (memory banks) [figure 3]; a variable delay (adjustable delay 310) [figure 3]; and a latch (data latch 317) [figure 3]. Li also teaches wherein said variable delay is coupled to receive input from a data path and coupled to provide output to the latch [figure 3]: and wherein said latch is coupled to receive input from the variable delay and provide input to said logic circuit [figure 3]. Furthermore, Li also teaches a control circuit, said control circuit comprising: a register (load mode register) [figure 3 and col. 3 lines 63-66]; a repeater (register 320 - passes data through a logic circuit) [figure 4 and col. 4 lines 9-10]; a comparator (substituted for phase detector) [col. 4 lines 25-31]; a command detector (command decode 397);

Chao et al., U.S. Patent 6,748, 539 (hereinafter "Chao") teaches a device comprising a functional circuit, said functional circuit comprising a logic circuit (coupled to input data at pad

159) [figure 1]; and a variable delay (delay circuit 139 may be calibrated) [figure 1 and col. 4 lines 32-41]; a latch (latch 151) [figure 1]. Chao also teaches wherein said variable delay is coupled to receive input from a data path (from output data 145) and couple to provide output to the latch (via buffers 135 and 155) [figure 1]. Chao further teaches wherein said latch is coupled to receive input from the variable delay and provide input to said logic circuit (via buffers 135 and 155) [figure 1]. Chao also teaches a control circuit having a comparator (within the PLL).

Yang et al., U.S. Patent 6,418,537 (hereinafter "Chao") teaches a device comprising a functional circuit, said functional circuit comprising a logic circuit (inherently coupled to DATAOUT 330) [figure 1B]; a variable delay (capture latches and delay interpolator) [figure 1B and col. 3 lines 36-42]. Yang also teaches wherein said latch is coupled to receive input from said variable delay (a delay amount from delay interpolator) and provide input to said logic circuit (through line 315 and window select 600) [figure 1B and col. 3 lines 36-42].

Johnson et al., U.S. Patent 6,434,081 teaches a device comprising a functional circuit comprising a logic circuit (DRAMs 69 and 70); a variable delay (ring delay 57); and a latch (latch 59) [figure 4]. Johnson also teaches wherein said variable delay is coupled to receive input from a data path and coupled to provide output to the latch [figure 4]. Johnson further teaches wherein said latch is coupled to receive input from a data path and coupled to provide output to the latch [figure 4]. Johnson also teaches a control circuit with register (logic 81 and 87) and a comparator (comparators 73a-73c and 83a-83b).

Sparks et al., U.S. Patent 6,028,898 teaches a device comprising a functional circuit further comprising a logic circuit (logic to re-timed data), a variable delay (adjustable delay 6) and a latch (latch 15) [figure 1 and col. 6 lines 29-61]. Sparks further teaches wherein said

variable delay is coupled to receive input from a data path (from buffers 10 and 11) and coupled to provide output to the latch [figure 1 and col. 6 lines 29-61].

Reazeanu, U.S. Patent 6,081,475 teaches a system that uses adjustable delays for delay equalization during writing of data.

Lee et al., U.S. Patent 6,374,361 teaches a system that uses variable delay to adjust data skew when transferring data between devices.

Applicants admitted prior art teaches a device comprising a functional circuit further comprising a logic circuit (DRAM devices), a variable delay (adjusting the timing of the received data bits) [pages 1 and 2].

The prior art of record does not teach or suggest individually or in combination wherein the register is coupled to receive input from a first external source and coupled to provide output to said repeater and said comparator. The prior art of record also does not teach or suggest individually or in combination wherein said repeater is coupled to receive input from said register and said command detector and to provide output to a second external source. Further, the prior art of record also does not teach or suggest individually or in combination wherein and said command detector is coupled to receive input from said second external source and to provide output to said repeater and said comparator. Lastly, the prior art of record also does not teach or suggest individually or in combination wherein said comparator is coupled to receive input from said latch of said functional circuit and said register and provide output to control said variable delay.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue

fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

EXAMINER'S AMENDMENT

5. An examiner's amendment to the record appears below. Should changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Christopher Chow, Reg. No. 46,493 on August 25, 2004.

The application has been amended as follows:

In the claims:

a. Claim 188, cancel claim 188.

b. Claim 189:

   i. line 1, replace "188" with --187--.

c. Claim 191:

   i. line 1, replace "198" with -- 187--.

Pursuant to MPEP 606.01, the title has been changed to read:

-- DEVICE AND SYSTEM FOR ADJUSTING DELAY IN A DATA PATH BASED ON COMPARISON OF DATA FROM A LATCH AND DATA FROM A REGISTER --

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James K. Trujillo whose telephone number is (703) 308-6291 [new phone number may be in effect in mid October - (571) 272-3677]. The examiner can normally be reached on M-F (7:30 am - 5:00 pm) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (703) 308-1159 [new phone number may be in effect in mid October - (571) 272-3670]. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James Trujillo
August 25, 2004

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 3600 2/00